Custom Design for Defense Operations

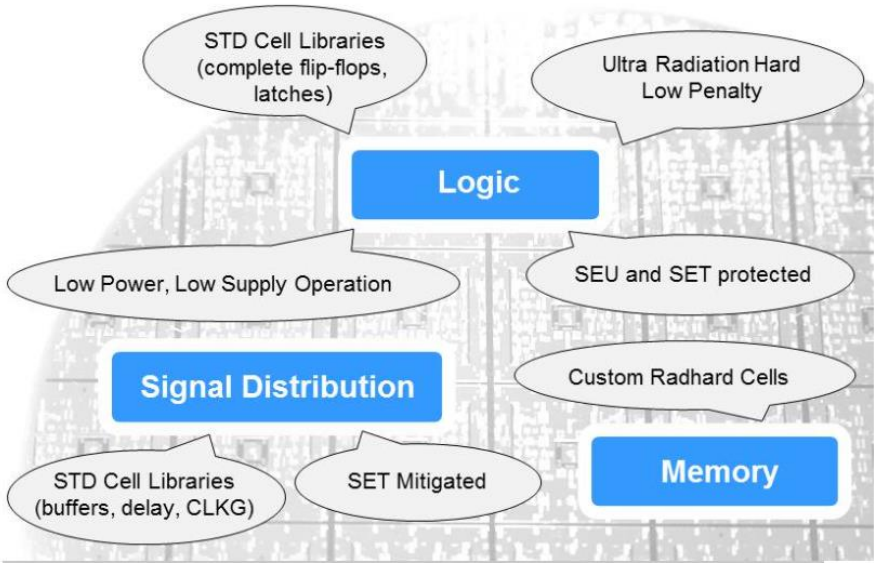
Our Custom Design for Defense Operations is engineered to meet the unique demands of next-generation nuclear modernization efforts and complex defense systems. Our custom design solutions leverage advanced methodologies like Layout design through Error Aware Positioning (LEAP). These solutions include layout and circuit optimization to reduce SER (Soft Error Rate) and latch-up sensitivity, ensuring resilient performance in the most challenging environments. Our expertise in designing radiation-hardened sequential and combinatorial logic cells, as well as memory cells, empowers mission-critical systems with precision, reliability, and durability.

The JRC Robust Chip Platform applies a unique Radiation-Hardened by Design (RHBD) technique using LEAP to design ultra radiation hard, low penalty, standard cells. Our standard cell library also contains unique flip-flop families for reduced switching power, and for operation at reduced supply conditions.

The ultra-low SER, low penalty (and low power) properties of JRC's LEAP-based standard cells have been verified experimentally in over ten different technologies, including bulk technologies from 180nm to 20nm, PDSOI and FDSOI technologies, and FinFET technologies (16nm, 12nm, 3nm).

Full library extensions are currently available for Global Foundries' 12LP and 12LP+ (RCP release 6.0) and Global Foundries' 32SOI (RCP release 4.0). Subsets of radiation hard cells (for 180, 28, 20nm bulk, 16, 7, 5, and 3nm FinFET, 28, 22nm FDSOI), or custom designs, are available in other technologies from 180nm to 3nm.

With a focus on interoperability, these custom solutions are designed with state-of-the-art capabilities to support the Department of Defense's most critical initiatives. Designed for extreme environments and critical applications, our advanced semiconductor technologies provide enhanced reliability and performance.

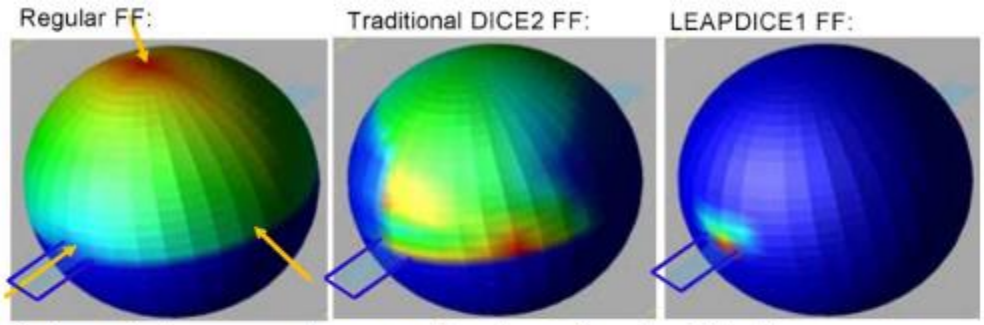


LEAP

JRC's efficient, layout-based, radhard-by-design methodology

LEAP (Layout design through Error Aware Positioning) is a unique layout methodology from JRC which can reduce single event generated soft error rates dramatically (up to several orders of magnitude), with negligible performance and area penalties.

The efficacy of LEAP has been experimentally verified for flip-flops in bulk semiconductor technologies (180-20nm), SOI technologies (32, 28nm), and FinFET technologies (16, 14, 5, and 3nm).



Color-coded cross-section as a function of angle of incidence at LET = 15 MeVcm^{2}mg^{-1}.

OVERVIEW OF ERROR RATE IMPROVEMENT AND PENALTIES FOR LEAP IN ADVANCED BULK TECHNOLOGIES

	Speed	Power	Area	SEU rate (UDSM bulk)
Trad. regular FF	1	1	1	1
LEAP regular FF	~1.1	~1.1	~1.1	0.2-0.7
Traditional layout redundant (trad. DICE)	1	~1.6	1.8-2	~0.1
LEAP layout redundant (LEAPDICE)	~1.02	~1.63	1.8-2.2	10^{-3} - 10^{-5}

Although the implementation of the LEAP methodology is more complex, it can be implemented, in most technologies, in a way that is fully compatible with traditional layout styles. The LEAP based logic cells in JRC's standard cell library extensions can be freely mixed with regular (traditional layout) standard cells (of the same height).

Both sequential and combinatorial logic has been successfully implemented using LEAP (and experimentally verified). The technique has been developed with support from the Defense Threat Reduction Agency. It is patent protected.

The JRC engineering team has successfully applied the LEAP design methodology and JRC's analysis tools in numerous designs and projects over many years. Our service offer is a way for clients to get radiation hard logic cells in addition to the physical IP offered by JRC, or to get

accurate predictions for, and insight, into the soft error and latch-up behavior for specific circuits and layouts.

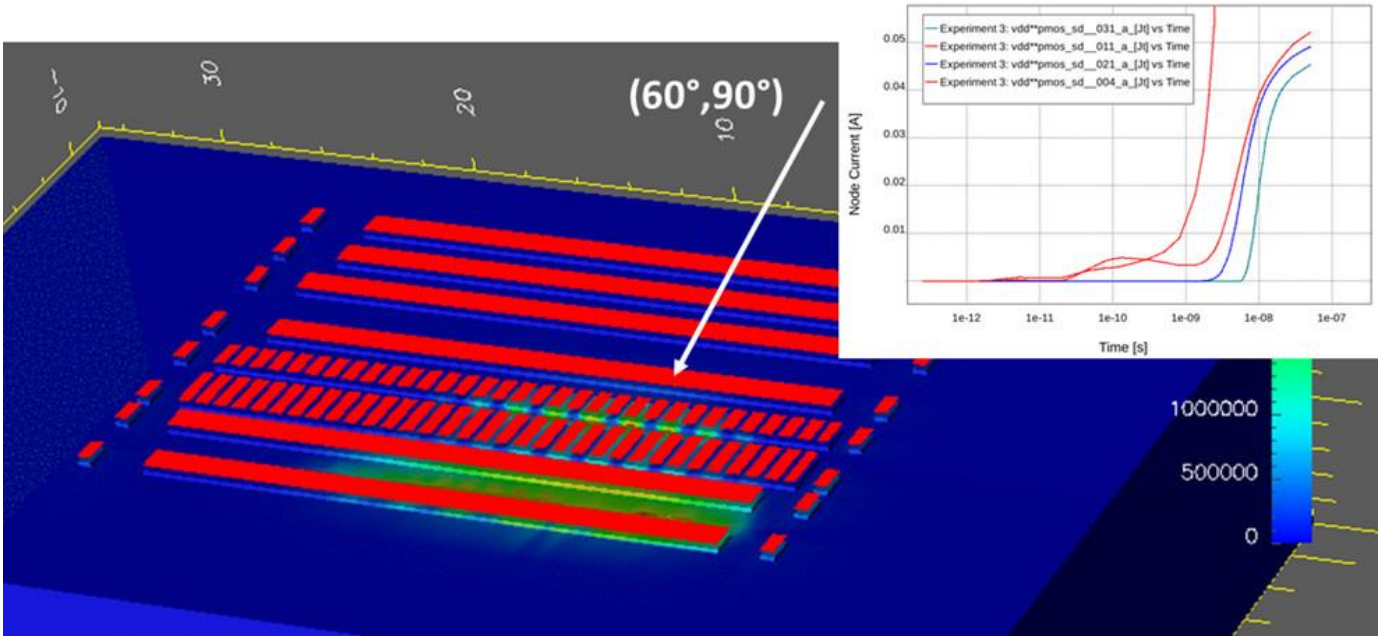
Physical IP and Custom Design Support Services

Soft Error and Latch-up Evaluation

Prediction of SER and latch-up rates, custom SER hard logic cells, and general simulation projects:

Dedicated simulation projects providing SEU, MBU, SET, and/or latch-up rates, and full insight into the single event behavior can be performed. The analysis will identify potential weaknesses related to single events and provide sufficient explanation and suggestions to fix them.

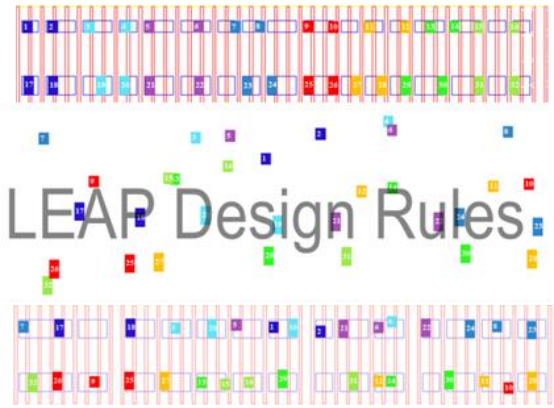
Typical target circuits are flip-flops, latches, and SRAM memory. Other applications include combinatorial cells (for logic or signal distribution), hardened circuits (e.g., TMR), DRAM, FPGA switches, ESD circuits, and high voltage devices.



LEAP Design Rules

Optimizing Resilience

The image below illustrates how LEAP applies structured, error-aware positioning to mitigate radiation-induced faults while maintaining efficiency.



Radiation-induced Error Rate Estimates for Standard Cell Libraries

The image below represents a radiation impact simulation on standard cell layouts, highlighting sensitive regions vulnerable to Singel Event Effects (SEEs). The color-coded heatmap overlays the circuit layout, indicating areas with higher susceptibility to radiation-induced disruptions.

- Single Event Upset (SEU) and Single Event Transient (SET) rate estimates for standard cell libraries
- Multi-Bit Upset (MBU) and Multiple Cell Upset (MCU) sensitivity analysis for SRAM and logic circuits
- Soft Error Rate (SER) evaluation across diverse process nodes
- Comprehensive Design Resilience (DR) estimates for large-scale logic circuits