LEAP Standard Cell Libraries and Custom Logic Cells

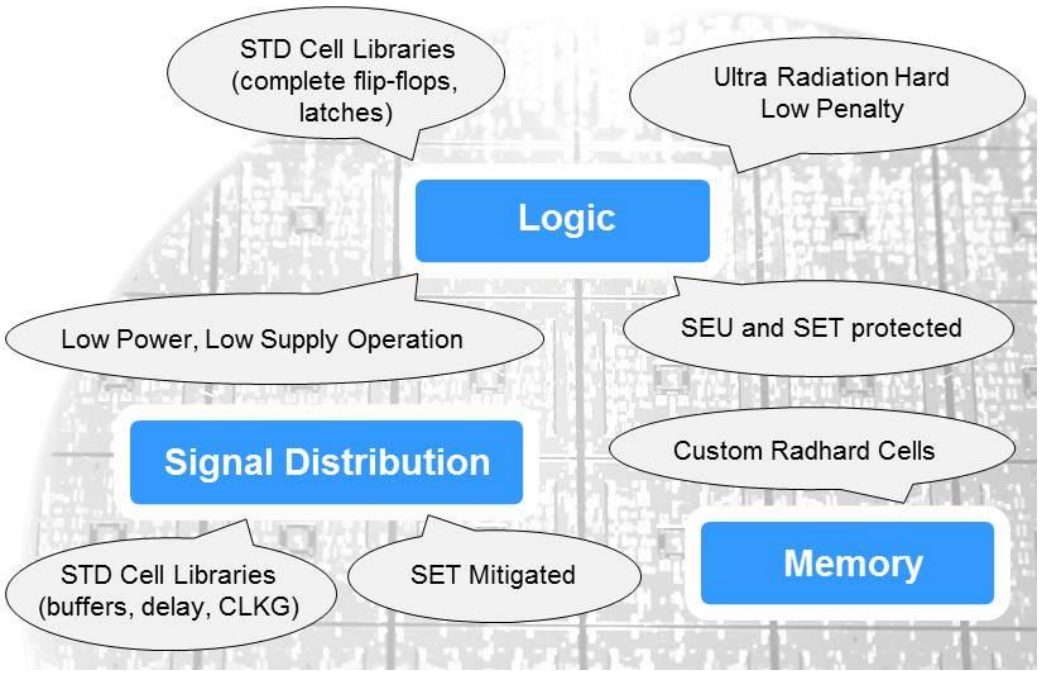
Efficient hardening against soft errors for low power design

JRC's Robust Chip Platform's patented standard cell library enables modern semiconductor foundries to deliver cutting -edge solutions for critical aerospace and defense missions. Harnessing advanced techniques for radiation modeling, the JRC robust Chip Platform offers unmatched accuracy in radiation error rate analysis for standard cell libraries.

Tested under the most extreme conditions, our technology ensures unparalleled performance, operational longevity, and success in demanding aerospace defense environments.

JRC's Robust Chip logic cells are fully compatible with regular (commercial) standard cell libraries. Integration of these cells is seamless and can be done selectively at critical locations in a design, or by replacing all cells. All cells are provided with complete EDA views (gds, netlist, lef, liberty, verilog).

Our library extensions contain several families of low energy and area-efficient SER hard (redundant) flip-flops and latches, a family of low power, SER mitigated (non-redundant) flip-flops, and a set of set mitigated cells for clock and signal distribution. All flip-flops are available with scan, and asynchronous preset/clear functions.



All logic cells have been designed using JRC's unique RHBD technique, Layout Design through Error Aware Positioning (LEAP), which provides dramatic SER reductions with minimal penalties. Furthermore, sequential logic cells designed using the LEAP technique have been proven to maintain their very low SER at low supply conditions (down to near threshold) more efficiently than regular (not hardened) cells. The LEAP technique has been experimentally verified in a long range of semiconductor technologies (bulk, SOI, and FinFET technologies ranging from 180nm to 3nm).

A complete core STD cell library is available for Global Foundries' 12LP technology. Subsets of radiation hard logic cells are available in 180, 28, 20nm bulk, 16, 7, 5, 3nm FinFET, and 28, 22nm FDSOI. Custom designs are available in other technologies from 180nm to 3nm.

LIBRARY EXTENSION SUMMARY										
	Circuit	LEAP	Function[1]			Power[2]	Area[2]	SER[2]	SET mit.	SET prot
Flip-flop families		RHBD	S	P	C					
LEAPDICE0	DICE clocked-INV	x	x	x	x	2x	2x	0.0001x		[3]
LEAPDICE1	DICE clocked-INV	x	x	x	x	2x	2x	0.0001x	x	[3]
LEAPDICE2	DICE clocked-INV	x	x	x	x	2x	2x	0.0001x	x	[3]
LEAPDICE40	DICE low power	x	x	x	x	0.5-2x	2x	0.0001x	x	[3]
DFF40	DFF low power	x	x	x	x	0.2-0.8x	1.1x	0.5x		
Latches										
(please see datasheets)		x				2x	2x	0.0001x		[3]
CLK/signal distr.										
BUFH	Buffers	x				1x	1.5x	n/a	x	n/a
DLYH	Delay cells	x				1x	1.5x	n/a	x	n/a
Clock-gating	Clock gating cell	x				1x	2x	0.0001x	x	[3]

[1] *Scan (S) and asyncronous preset (P) and clear (C). Combined preset and clear (PC) are available except for LEAPDICE40.*

[2] *Approximate power, area, and SER relative to a typical regular (not redundant or hardened) cell (see the datasheets).*

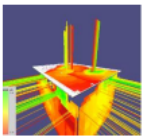
[3] *Flip-flop versions with redundancy-in-time SET filtering will be included in the next releases of the 32nm and 14nm libraries.*

Radiation Hard, Low Power Libraries

Radiation Hard, Low Power Standard Cell Library in GF12LP (12nm FinFET)

JRC's radhard, low power standard cell library release 2:

- Complete radhard and low power sequential logic cells (flip-flops and latches).
- Complete radhard logic cells for signal distribution (clock gating, buffer, delay cells).
- Error rate: 10^{-3} to 10^{-5} vs regular (not hardened) cells.
- Low power flip-flops: power reduction ~30% vs. other high-speed flip-flops.
- Complementing sets of DECAP and FILL cells.
- Fully compatible with cells from other commercial standard cell libs.



JRC's radhard, low power, standard cell library release 3:

- Complete set of (regular) core logic cells.
- Additional radhard combinatorial and sequential cells (including INVH, LVLSH, LEAP341F, and 2-bit and 4-bit radhard flip-flops and latches).

JRC's radhard, low power, standard cell library release 4:

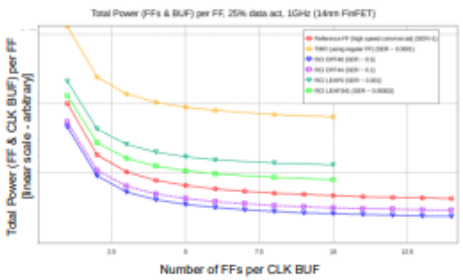
- Complementing radhard cells (including negative edge versions for key radhard FF families, additional multibit-FFs, and additional SET filter capabilities).

JRC's radhard, low power, standard cell library release 6:

- Complementing radhard cells (including additional FF families with both SEU and SET protection, additional multibit-FFs, radhard synchronizer FFs, radhard Clock-MUXes, and additional SET mitigated combinatorial cells for signal distribution).

The radiation hard STD cell library is provided with complete EDA views and with SEU rate and SET pulse rate estimates for eight different radiation environments for all cells. Release 2 contains 4620 cells, release 3 over 8000 logic cells, and release 6 more than 12,000 cells. All cells are verified in silicon (release 3 and 4 final in-silicon in Q4 2021). The library is in 9T cell height, and the cells can abut to, i.e., be mixed with, logic cells from other commercial libraries in 9T (several versions available). All key radhard cells have been radiation tested, verifying error rate reductions both at nominal supply conditions and down to near threshold operation.

Selected radhard library cells		Rel.	Function	Power	Area	SER
LEAP1	LEAP DICE	2	Scan, PRST, CLR	2x	2x	0.0001x
LEAP341	low power LEAP DICE	2	Scan, PRST, CLR	0.5-2x	2.3x	0.00001x
DFF40	low power DFF	2	Scan, PRST, CLR	0.2-0.8x	1.1x	0.5x
DFF45	low power DFF	3	Scan, PRST, CLR	0.4-1.4x	1.2x	0.15x
CLKG	LEAP DICE	2	clock gating	2x	2x	0.0001x
leap_latch	LEAP DICE	2	PRST,CLR	2x	2x	0.0001x
BUFH, DLYH	buffer, delay	2		1x	1.5x	0.02x
INVH	inverter	3		1x	1.2x	0.5-0.1x
LEAP341F	low power LEAP DICE	3	Addl rad protect	0.5-2x	2.7-3.5x	0.00001x
LVLSH	level shifter	3	SET protection	2x	2x	0.001x



Radiation Hard, Low Power Logic Cells in Other Technologies

A smaller set of radhard and low power cells, as well as custom designed cells, are available in 3nm, 5nm, 7nm and 16nm FinFET, in 22nm and 28nm FDSOI, in 32nm PDSOI, and in 20, 28, and 180nm bulk technologies.